REMARKS

Claims 1 – 30 remain in the application. Claims 1 – 30 stand rejected. Claim 30 is objected to. Claims 1, 12, 13, 19, 29 and 30 are amended herein. The rejection of claims 1 – 30 is respectfully traversed.

The specification is objected to for containing informalities. Responsive thereto, pages 1 and 9 are amended herein as directed by the Examiner. Reconsideration and withdrawal of the objection to the specification is respectfully solicited.

Amendments to claims 1 and 12 are supported by the specification as filed and by claims 13 and 30. Claim 19 was amended to correct informalities therein. No new matter has been added.

Claim 30 is objected to because "it appears that claim 30 should depend from claim 19 instead of 18 and 'Vddl' appears to be --Vddh--." While claim 30 should indeed have depended from claim 19, claim 30 correctly recites "V_{ddl}." Claims 19 – 30 are directed to an Integrated Circuit (IC) e.g., as illustrated in Figure 4 and described on page 9, line 5 – page 10, line 15. With the reduced supply voltage below V_{ddl}, PFET 114 in Figure 1A and B and PFETs 148, 150 in Figure 2 turn off hard because V_{gs} is positive as described on page 7, lines 1 – 23. Accordingly, claim 30 is amended herein to correct dependency as directed by the Examiner. Reconsideration and withdrawal of the objection to claim 30 is respectfully solicited.

Claims 11, 17 and 29 are rejected under 35 U.S.C. §112 for failing to provide antecedent basis for terms recited therein. Responsive thereto, claims 11, 17 and 29 have been amended herein. Reconsideration and withdrawal of the rejection of claims 11, 17 and 29 under 35 U.S.C. §112 is respectfully solicited.

Claims 1 – 10, 12 – 16 and 18 – 28 are rejected under 35 U.S.C. §§102(b) and 103(a) over E.P. 125,733 to Feller. The rejection is respectfully traversed.

Feller teaches a level translator circuit for interfacing bipolar, Transistor to Transistor Logic (TTL) to CMOS. *See, e.g.*, Feller Abstract and page 2, line 34 – page 4, line 36. Feller recites that the "CMOS circuit has to be controlled by signals on TTL

level (high level 2.0 V; low level 0.8 V) produced by TTL circuits," at page 3, lines 15 – 17. To date, as far as the applicants are aware, TTL circuits are not integrated on CMOS chips or vice versa. Thus, the Feller circuit is interfacing a TTL circuit or chip with a completely separate CMOS circuit or chip. Since Feller does not specifically recite device thresholds, one must conclude that Feller was in typical CMOS technology. In typical CMOS technology, thresholds are selected for PFETs and NFETs to have approximately equal magnitude. Typical device thresholds for 1 micron (1μ) CMOS in 1984, at the time of filing/publication of Feller, were 1.0 – 1.5 volts, e.g., +1.4V for the NFET and –1.4V for the PFET. These thresholds are at or near the midpoint between the TTL logic levels, which makes these thresholds desirable for maximum noise margin (2.0V – 0.6V and 0.8V +0.6V). So in Figure 2d, for example, with both inputs at 2.0V, N1, N2, N4, are on and P4 is off; Node D is at about Vdd – V_{TN}, 5 – 1.4 =3.6V; P1 and P2 are on, albeit softly, i.e., for P1, V_{SG} = 3.6V – 2.0V = 1.6V > 1.4V. So, current flows continuously with both inputs high and the circuit dissipates static standby power.

Claims 1 and 12 are amended to recite that "standby power is substantially eliminated" in the level converter when the input/output is high. This is not taught nor suggested by Feller. Claim 19 is drawn to an IC with high and low voltage circuits in the IC being interfaced by such a level converter, which Feller neither discloses nor suggests. Therefore, Feller does not teach or suggest the present invention as recited in claims 1, 12, or 19. Reconsideration and withdrawal of the rejection of claims 1, 12, and 19 under 35 U.S.C. §102(b) over Feller is respectfully solicited.

Furthermore, because dependent claims include all of the differences with the prior art as the claims from which they depend, Feller does not teach or suggest the present invention as recited in any of claims 2 – 10, 13 – 16, 18 or 20 – 28, which depend from claims 1, 12, and 19. The applicants note that claims 11, 17, and 29 have not yet been substantively rejected. Reconsideration and withdrawal of the rejection of claims 2 – 10, 13 – 16, 18 and 20 – 28 under 35 U.S.C. §§102(b) and 103(a) over Feller is respectfully solicited.

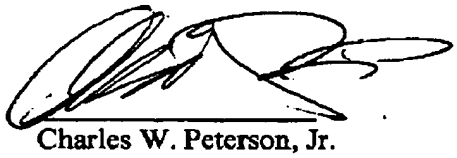
The applicants have considered the other references cited but not relied upon and find them to be no more relevant than Feller.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons set forth above, the applicants respectfully request that the Examiner, reconsider and withdraw the objection to the specification and claims, reconsider and withdraw the rejection of claims 1 – 30 under 35 U.S.C. §§102(b), 103(a) and 112 and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,



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